CBSC pipelined ADC with comparator preset, and comparator delay compensation

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***Abstract*—We present a differential comparator-based switched-capacitor (CBSC) pipelined ADC with comparator preset, and comparator delay compensation. Compensating for the comparator delay by digitally adjusting the comparator threshold improves the ADC resolution 23 times. The ADC is manufactured in a 90nm CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for the input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5mW at 60MS/s.**

I. Introduction

The downscaling of CMOS technology continues to challenge the analog designer. With a power supply of 1.2V in 90nm CMOS technology, and a threshold voltage up to 0.5V in a low-power flavor there is not much headroom to stack transistors, and when the transistor intrinsic gain[1] worsens with each technology node (down to an amplification of around 16 times in 90nm) it makes a high performance operational transconductance amplifier (OTA) really hard to design. This is bad because OTAs are the key component in most switched-capacitor circuits, and switched-capacitor circuits are almost the de facto standard for implementing analog to digital converters (ADCs). This has caused a flurry of research into removing the OTA, where one of the research avenues has led to the comparator-based switched-capacitor circuits (CBSC) [1].

A simplified model of a switched-capacitor circuit can be seen in fig. 1. It has two phases, sampling and charge transfer. In sampling the input voltage is stored as a charge on two capacitors. During charge transfer the charge from C_1 is transferred to C_2, this implements a gain of two if the capacitors have the same value. Shown in the figure are the charges across the capacitors at $t = 0$, the start of charge transfer, and at $t = 0.5/f_s$, the end of charge transfer (f_s is the sampling frequency).

The function $f(x)$ ensures that the charge across C_1 is equal to zero at the end of charge transfer. The conventional method uses an OTA with a large open-loop gain to force zero charge across C_1 by forcing the voltage at node 1 to zero. But CBSC does it differently, it first forces the output voltage to the lowest voltage in the circuit, then it charges the output node with a constant current. This causes the output voltage to rise, much like a ramp, and when the comparator (connected to the inputs of $f(x)$) detects a zero voltage at node 1 the current is turned off.

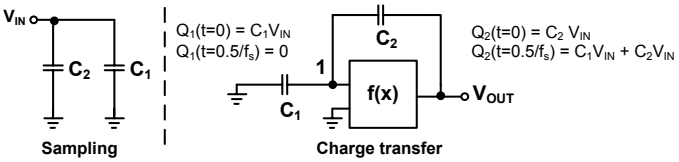


Fig. 1. Principle of a switched-capacitor circuit.

One of the key challenges in CBSC is the comparator delay. Since any real comparator has a delay, it takes a moment for the current source to turn off, accordingly the output voltage overshoots.

Methods to compensate for this overshoot exists, in [2] they used a dual ramp system, first a fast ramp to estimate the output voltage, then a slow ramp to fine tune the output voltage. Since the ramp was slow the comparator delay caused an insignificant voltage change. A dual ramp system was also used in [3], but they included an additional compensation for overshoot using a switched-capacitor circuit. In [4] an analog signal was globally adjusted to compensate for the offset of the ADC. The scheme used in [5] (presented febuary 2009) is similar to the scheme used in our ADC, but we present a method that simplifies the comparator logic by ensuring the state of the comparator is known before and after charge transfer, and we compensate for the comparator delay by digitally changing the comparator threshold with a different scheme.

This paper is organized as follows, the circuit implementation is explained in section II and in section III we present the measurement results.

II. Implementation

A system level diagram of the ADC is shown in fig. 2. It has seven 1.5-bit pipelined stages and a 1.5-bit flash-ADC.[2] The circuit implementation of each block is detailed in the following sections.

A. Pipelined stage

Stage 1 is shown in fig. 3 during sampling and charge transfer. Stages 2-7 are identical to stage 1 with the exception

[1]The intrinsic gain is the transconductance times the output resistance, or g_m/g_{ds}.

[2]The ADC was designed as a 10-bit ADC with eight 1.5-bit stages and a 2 bit flash-ADC. But measurements showed more noise than expected (the noise was dominated by the the digital IO). Accordingly, stage 8 was turned off and the output of the flash-ADC ignored.

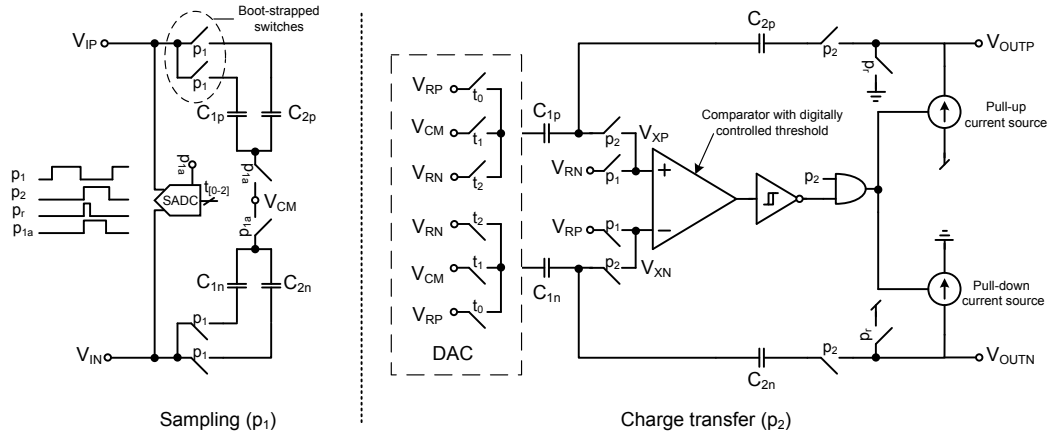


Fig. 3. Stage one shown during the two phases, sampling and charge transfer.

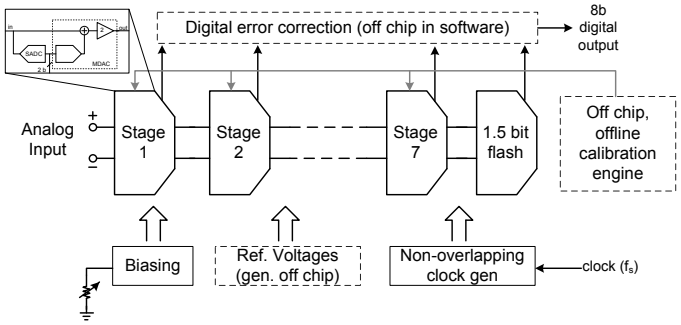


Fig. 2. System level diagram of the pipelined ADC.

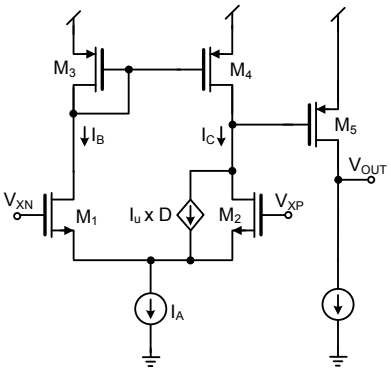


Fig. 4. Comparator with adjustable threshold.

of the input switches and capacitor size. The input switches are boot-strapped in the first stage, but regular transmission gates in later stages.

Each stage has a 1.5-bit analog-to-digital converter (SADC). The 1.5-bit stage uses redundancy to correct for offset errors in SADC comparators [6]. As a result, dynamic comparators can be used, which have large offsets but consume little power. In this converter the resistive divider dynamic comparator was used [7]. The signals t_0, t_1 and t_2 are the thermometer encoded digital output of the SADC.

The stage operates on four clock phases p_1, p_2, p_r and p_{1a}. An advanced (as in transitions before) clock phase (p_{1a}) samples the input signal before p_1 turns off, this reduces the problem of signal dependent charge injection from p_1 switches.

The voltages V_{CM}, V_{RN}, V_{RP} are the common mode voltage, negative reference voltage, and positive reference voltage respectively.

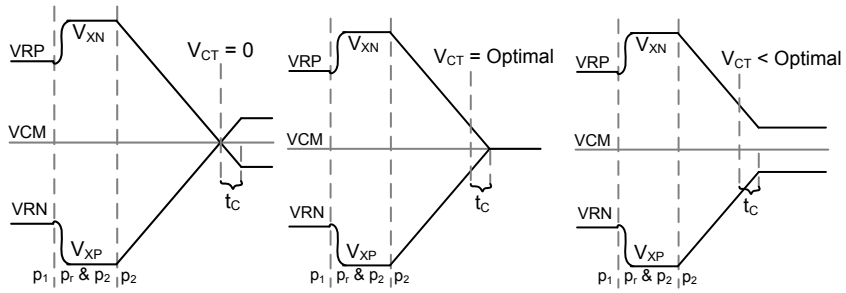
1) Comparator with adjustable threshold: A two-stage continuous time amplifier (fig. 4) with a differential first stage and single ended common source second stage is used as the comparator.

In phase p_1 the comparator inputs are reset to V_{RN} and V_{RP} (as shown in fig. 3), so the output is known at the end of p_1. With this preset the control logic to turn off the current source at the right time consist of a single Schmitt trigger and an AND gate. The preset also ensures that the comparator does not need to slew when we enter phase p_2, where we have very little time to do any more than strictly necessary.

In phase p_2 the stage outputs are reset (p_r), forcing a slight increase in V_{XN} and decrease in V_{XP}, the amount of change depends on the stage input voltage (see fig. 5 for a visualization). When reset is complete (p_r goes low) the current sources start charging the stage outputs. As a result V_{XN} falls and V_{XP} rises, and when they meet we want to turn off the current sources, because that is when we have zero charge across capacitors C_{1p} and C_{1n} (assuming the DAC output is connected to V_{CM}), and all the charge is transferred to C_{2p} and C_{2n}.

Fig. 5(a), fig. 5(b), and fig. 5(c) shows V_{XN} and V_{XP} as a function of time for different comparator thresholds (V_{ct}). The comparator should turn off current sources when $V_{XP} = V_{XN}$, but because the comparator has a delay (t_c) the current sources turn off later, causing an overshoot (fig. 5(a)). Adjusting the threshold of the comparator changes the amount of overshoot. If V_{ct} is adjusted optimally there is no overshoot (fig. 5(b)). If V_{ct} is lower than the optimal value the output undershoots (fig. 5(c)). From the figure we see that a non-optimal threshold cause an offset in the stage output, as shown in [8].

To control the comparator threshold we use a 6-bit current



(a) Comparator threshold equal to zero (b) Optimal comparator threshold (c) Comparator threshold less than the optimal value

Fig. 5. Voltage versus time for the nodes V_{XN} and V_{XP} as a function of comparator threshold.

DAC in parallel with M_2, shown as a controlled source in fig. 4. In the figure I_u is a unit current and D is an integer given by $D = 2^0b_0 + 2^1b_1 + 2^2b_2 + 2^3b_3 + 2^4b_4 + 2^5b_5$. The current in the current source I_A is the sum of the two branch currents ($I_A = I_B + I_C$). The comparator threshold is defined as the differential input voltage when the branch currents are equal ($I_B = I_C$). Equal currents occur when

$$\beta V_{EFF,1}^2 = \beta V_{EFF,2}^2 + I_u \times D \tag{1}$$

where $\beta = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ and $V_{EFF,1|2}$ is the effective gate overdrive of transistors $M_{1|2}$ [3]. If $D = 0$ the currents are equal when the effective gate overdrive's are equal, which occurs when the inputs are equal. If $D > 0$ the currents are equal when the effective overdrive of M_1 is larger than the effective overdrive of M_2, which occurs when $V_{IN} > V_{IP}$.

The nominal delay of the comparator (including Schmitt trigger and logic gates) is $t_c = 0.5ns$. With the 6-bit DAC the effective delay of the comparator can be controlled from $t_c = -0.9ns$ to $t_c = 0.5ns$.

2) Boot-strapped switches: The input switches in the first stage of a pipelined converter feel the full force of a sinusoidal input signal, which means that the voltage dependent switch resistance does make a difference to the linearity of the converter. So in the first stage it is common to use special switches, and we've used a type of continuous time boot-strapped switches [9]. This is especially relevant in nano-scale technologies since low resistance switches have become harder to design due to the lowered headroom.

3) Current sources: We used wide-swing regulated cascode current sources to achieve high output resistance in the current sources. A PMOS current source was used for the pull-up current (see fig. 3), and a NMOS current source was used for the pull-down current. The current in the current sources can be digitally controlled.

B. Other

External reference voltages were used for testability, so the power consumed by the references is not included in reported power dissipation. The digital outputs from the SADCs are brought off-chip by CMOS logic IO buffers. Synchronization, recombination and digital error correction of the output bits was performed in software.

[3]Here we assume a square law model for the transistors, and that the transistors are in strong inversion and saturation

III. Measurement results

The essence of this paper is the preset to simplify the logic after the comparator, and the comparator delay compensation by digitally adjusting the comparator threshold. The development of an efficient calibration algorithm has been left for future research.

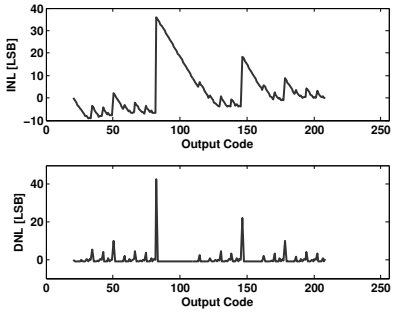
The optimum comparator threshold and current source current was found using a simple calibration algorithm, the algorithm is detailed in [8].

With the default comparator threshold and current source current set before production the offset caused by overshoot is excessive, as a result the maximum integral non-linearity (INL) is 36 LSB (seen in fig. 6(a)), and the ADC has an ENOB of 2.5-bit. After calibration, with optimal comparator threshold and current source current the ADC has an ENOB of 7.05-bit and a maximum INL of 0.7 LSB (this might be difficult to see from fig. 6(b), but the same axis as fig. 6(a) has been used to avoid confusion). This is an improvement of 23 times (2.5-bit to 7.05-bit), which demonstrates the variations caused by processing can be canceled by digitally adjusting the threshold of the comparator. The adjustment of current source current contributed to a lesser degree to the improvement in the resolution (around 0.5-bit).

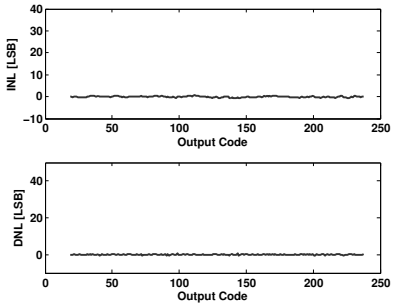
A summary of the ADC performance is shown in Table I. It achieves a *signal-to-noise and distortion ratio* (SNDR) of 44.2-dB (7.05-bit) with a sampling frequency (f_s) of 60MS/s, an input signal of $f_s/2$, and a power dissipation of 8.5mW (5.9mW for ADC core, 2.3mW for clock generation and distribution, and 0.3mW for input switches), which results in a Walden figure of merit of 1.07 pJ/step[4] and a Thermal figure of merit [8] of 8.09fJ/step.[5] An input signal amplitude of -1 dBFS was used during measurement.

The ADC has a *spurious free dynamic range* (SFDR) of 60-dB at $f_s/2$. The SNDR and SNR change little with input frequency, and the effective resolution bandwidth extend well beyond $f_s/2$ (as seen in fig. 8).

[4]$FOM = P/2^B f_s$
[5]$FOM = P/2^{2B} f_s$



(a) No calibration, default values set before before production.



(b) After calibration of comparator offset and current source current

Fig. 6. INL and DNL for uncalibrated, and calibrated ADC

A 8192 point FFT of the ADC output is shown in fig. 7. Coherent sampling and a Hanning window was used to avoid spectral leakage.

Compared to state-of-the-art CBSC converters with similar resolution and speed [4] we have around 2.8 times worse figure-of-merit (1.07pJ/step vs 0.38pJ/step), but [4] was manufactured in a 0.18μm CMOS technology, while our ADC was manufactured in a 90nm CMOS technology.

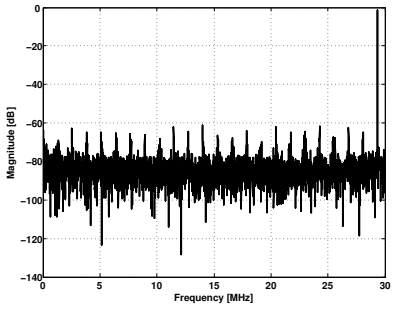


Fig. 7. A 8192 point FFT of the ADC output

IV. Conclusion

We presented a differential comparator-based switched-capacitor (CBSC) pipelined ADC with comparator preset, and comparator delay compensation. Compensating for the comparator delay by digitally adjusting the comparator threshold improved the ADC resolution 23 times. The ADC was manufactured in a 90nm CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for the input switches. The ADC had an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5mW at 60MS/s.

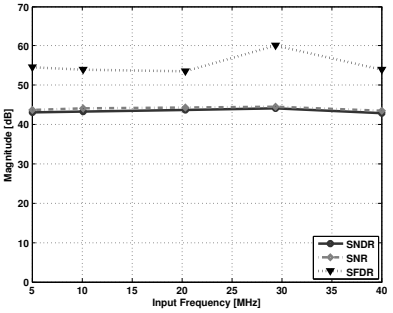


Fig. 8. SNDR, SNR and SFDR versus frequency, sampling frequency is 60MS/s.

TABLE I
Summary of calibrated ADC performance

Full scale input	0.8V
DNL (LSB)	0.52 / -0.54
INL (LSB)	0.6 / -0.77
SNR (29.4MHz input)	44.5 dB
SNDR (29.4MHz input)	44.2 dB
SFDR (29.4MHz input)	60 dB
ADC core power	5.9mW
Clock power	2.3mW
Input switches (1.8V)	0.3mW

Acknowledgments

We thank professors David Johns and Ken Martin for their advice during design of the ADC, and thank the Electrical and Computer Engineering Department, University of Toronto for their hospitality during our stay. We thank Johnny Bjørnsen for help with measurements.

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