Design and behavioral simulation of comparator-based switched-capacitor circuits

Carsten Wulff , Trond Ytterdal
Department of Electronics and Telecommunication
Norwegian University of Science and Technology

***Abstract*—Design equations are a required tool in the analog designers toolbox. In this paper we show how one can calculate the required parameters for comparator-based switched-capacitor circuits for use in a pipelined ADC. The parameters are capacitance (C), current (I_0), comparator delay (T_d), current source output resistance (R_o) and comparator threshold (V_{ct}). The design equations are verified with behavioral simulations in SPICE and MATLAB.**

I. Introduction

Downscaling of CMOS technology continue to challenge the analog designer. Reduced power supply, due to reliability concerns [1], and reduced transistor output resistance, due to shorter channels [2], lead to low headroom and low intrinsic gain. As a consequence, high DC gain operational amplifiers (opamp) — the key component in most switched-capacitor circuits — is hard to design in nano-scale technologies.

Techniques like correlated level shifting [3], open-loop residue amplifiers [4], gain calibration [5], and comparator-based switched-capacitor circuits (CBSC) [6] have been developed to solve some of the challenges. The techniques either reduce the gain requirements for a given resolution, or replace the opamp completely.

Introduced in [6] CBSC is a completely new approach to switched-capacitor circuits. It replaces the opamp with a comparator and a current source. To demonstrate the technique a prototype 10-bit 8-MS/s 2.5-mW pipelined ADC was presented at ISSCC 2006 [6]. The implementation was detailed in [7].

In this paper we discuss how to design CBSC circuits for analog-to-digital converters.

Before one starts simulating transistors in SPICE it is of utmost importance to have a clear idea of the dominating error sources, and how they should be handled. In that respect, tools like design equations, mathematical simulations and behavioral SPICE simulations are invaluable tools for the analog designer.

a) Design Equations: Based on the specification (how fast, how accurate, how little power) the parameters for different circuit blocks can be calculated. The design equations result in a place to start, a set of initial parameters to work with.

b) Mathematics based simulation: Behavioral simulation in a mathematics based tool, like MATLAB or OCTAVE, is more complex than design equations, but more accurate. But it is still fast and a designer can sweep parameters to find optimal solutions.

c) SPICE simulation: Behavioral level description in SPICE allow the designer to have a top-level description of the circuit, with all circuit blocks defined. The functionality of circuit blocks is checked before circuit blocks are implemented with transistors.

This paper is organized as follows: Section II review opamp based switched-capacitor circuits. Section III explain comparator-based switched-capacitor circuits. A model of the output voltage of a CBSC amplifier with a gain of two is described in Section IV. In Section V we introduce a design methodology for CBSC circuits and show a design example in Section VI. Results of simulations in MATLAB and SPICE verify our design equations in Section VII.

II. Opamp based switched-capacitor circuits

Switched-capacitor (SC) circuits are usually designed with an opamp feedback loop as shown in Fig. 1. Most SC circuits have two clock phases, sampling and charge transfer. Fig. 1 is a amplifier where the input is sampled in phase p_1, and charge is transferred from C_1 to C_2 in p_2 by forcing V_x to ground. If the opamp has infinite gain the discrete time transfer function for Fig. 1 is a delayed amplification, where the gain is determined by the capacitance ratio.

$$H_0(z) = \frac{C_1 + C_2}{C_2} z^{-1} \tag{1}$$

With finite gain in the opamp the transfer function is

$$H_1(z) = H_0(z) \times \frac{1}{1 + (C_1/C_2 + 1)/A} \tag{2}$$

where A is the DC gain of the opamp. Finite gain in the opamp reduce the gain of the SC amplifier. For the remainder of this work we assume $C_1 = C_2$, so the amplifier has a gain of two.

III. Comparator-based switched-capacitor circuit

It does not matter how a SC circuit arrive at the output voltage. What matters is that the output voltage is correct when the next stage samples, which usually is at the end of charge transfer.

Instead of an opamp a current source and a comparator can be used [6]. An opamp forces the virtual ground condition while CBSC charge the output with a current source and detect when virtual ground is reached.

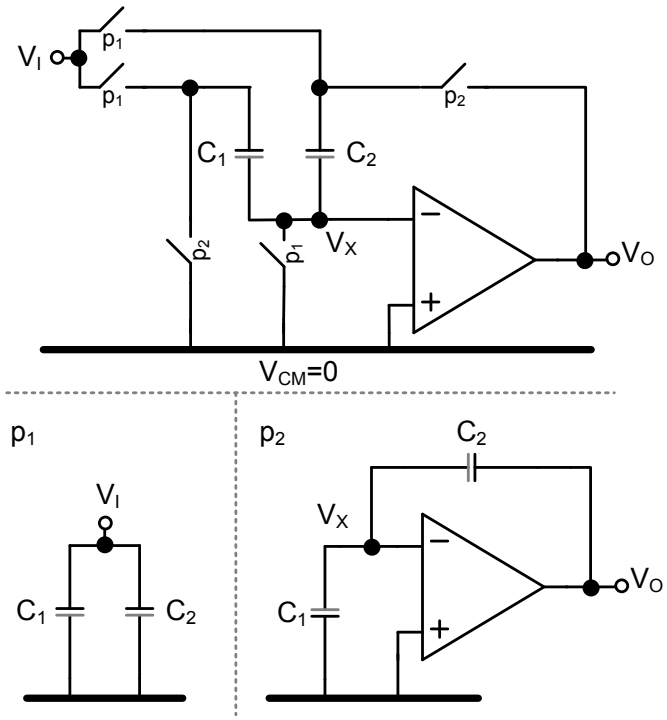

Fig. 1. Switched-capacitor amplifier using an operational amplifier

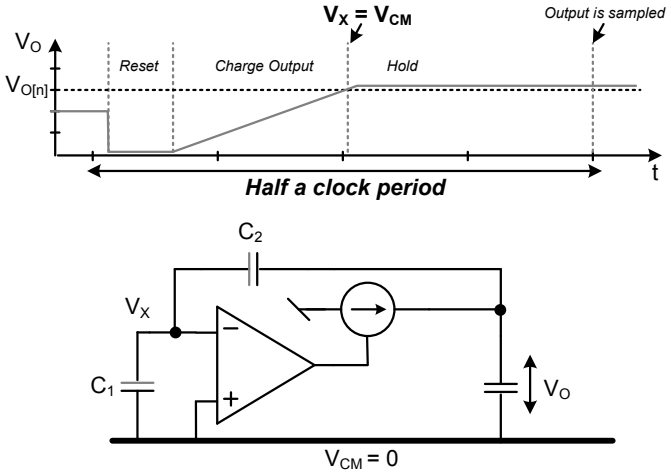

Fig. 2. Comparator-based switched-capacitor circuit

An example of a single ended CBSC is shown in Fig. 2, only charge transfer phase is shown, sampling phase is equivalent to opamp based SC.

At the start of charge transfer the output is reset to the lowest voltage in the system (usually the negative supply voltage), which ensure that V_x start below the virtual ground (common mode). The current source is turned on at the start of reset and use reset to settle. When reset ends the current source charge the output capacitance. The voltage at V_o and V_x rise until the comparator detects virtual ground ($V_x = V_{CM} = 0$). Due to the comparator delay it takes a moment for the current source to turn off, which result in an overshoot.

The overshoot can be corrected in several ways. One way is using two ramps [6], one fast and one slow, the fast ramp does an estimate of the output voltage, while a slow ramp in the opposite direction discharge the overshoot. Another is to change the threshold of the comparator to compensate for the overshoot [8].

A analytical model of the output voltage is presented in the next section.

IV. Model of CBSC output voltage

Assume finite resistance in current source. Kirchhoff's current law give the differential equation

$$I_0 = C_o \frac{dV_o(t)}{dt} + V_o(t)/R_o \tag{3}$$

where C_o is the capacitance at the output, V_o is the output voltage, I_0 is the current in the current source and R_o is the output resistance of the current source. Solving the differential equation yields.

$$V_o(t) = I_0 R_o \left(1 - e^{-\frac{t}{R_o C_o}}\right) \tag{4}$$

The time t is the sum of T_{V_I} — the time to charge to the ideal output voltage ($V_o(t) = 2V_I$) — and the comparator delay T_d. The ideal charge time T_{V_I} is given by

$$T_{V_I} = -ln\left(\frac{-2V_I}{R_o I_0} + 1\right) C_o R_o \tag{5}$$

To compensate for the comparator delay the comparator threshold (V_{ct}) can be changed, so the comparator start switching before $V_o = 2V_I$ is reached. Accordingly, the charge time can be written as

$$t = -ln\left(-2\frac{V_I - V_{ct}}{R_o I_0} + 1\right) C_o R_o + T_d \tag{6}$$

Inserting (6) in (4) results in

$$V_o(t) = 2e^{-\frac{T_d}{R_o C_o}} V_I + I_0 R_o [1 - e^{-\frac{T_d}{R_o C_o}} (1 + 2\frac{V_{ct}}{I_0 R_o})] \tag{7}$$

The gain in of the amplifier should be two, but from (7) we see the gain is smaller than two ($2e^{-T_d/R_o C_o}$).

This gain error will cause static non-linearities when a CBSC circuit is used in a pipelined ADC. The gain error is a function of the comparator delay, the output resistance and output capacitance. The last term in (7) is the overshoot.

In the next section we will use these equations to calculate the necessary parameters for a CBSC circuit.

V. CBSC design equations

The SC circuit in Fig. 2 finds use in pipelined ADCs in the multiplying digital-to-analog converter (MDAC) [9]. The necessary parameters for CBSC are capacitance (C), current source current (I_0), comparator delay (T_d), current source output resistance (R_o), and comparator threshold (V_{ct}).

The first thing we need to calculate is the necessary sampling capacitance given by [10]

$$C = a_1 \times \frac{48kT2^{2B}}{V_{PP}^2} \tag{8}$$

where a_1 is a constant larger than one, k is Boltzmann's constant, T is the temperature in Kelvin, B is the number of bits, and V_{PP} is the differential peak-to-peak signal swing.

To estimate the required current we assume that the output ramp is constant so

$$V_o = \frac{I_0}{C_o} t \tag{9}$$

The current in the current source is then calculated from

$$I_0 = \frac{C_o(V_{pp}/4 + V_{cm})}{\frac{1}{2f_s} - T_r} \tag{10}$$

where V_{cm} is the common mode voltage, f_s is the sampling frequency, T_r is the reset time and C_o is the output capacitance given by

$$C_o = \frac{C_1 C_2}{C_1 + C_2} + C_L \tag{11}$$

where $C_1 = C_2 = C/2$, and C_L is the capacitance of the next stage.

The comparator delay is chosen based on technology and noise properties [7].

The required output resistance of the current source is determined by the gain error from (7)

$$1 - \epsilon_g = e^{-T_d/R_o C_o} \tag{12}$$

where ϵ_g is the gain error. The required output resistance is then

$$R_o = \frac{-T_d}{ln(1-\epsilon_g)C_o} \tag{13}$$

The comparator threshold (V_{ct}) compensate for the overshoot from (7) given by

$$V_{off} = I_0 R_o \left[1 - e^{-\frac{T_d}{R_o C_o}} \left(1 + 2\frac{V_{ct}}{I_0 R_o} \right) \right] \tag{14}$$

Hence, the comparator threshold can be calculated from

$$V_{ct} = -1/2\, I_0\, R_o \left(1 - e^{\frac{T_d}{R_o C_o}} \right) \tag{15}$$

VI. Design example

As an example we use a 9-bit pipelined ADC running at 50MS/s. The target technology is 90nm CMOS with a power supply of 1.2V, the signal swing is 1V peak-to-peak differential.

The comparator in the CBSC circuit is the dominating noise source, and according to [7] it adds slightly more than two times the noise power of a single transistor. We choose $a_1 = 3$ to have some margin. With $T = 300K$ the capacitance is from (8)

$$C = 160fF \tag{16}$$

The current, calculated from (10), is

$$I_0 = 22\mu A \tag{17}$$

where we have used $V_{cm} = 0.6V$, a reset time of $T_r = 1ns$ and $f_s = 50MHz$. Allowing for a margin we choose $I_0 = 30\mu A$.

The current is proportional to C_o, which is highly process dependent parameter (20% variation). To rectify this a capacitance dependent bias current could be used [9].

The comparator delay (T_d) depend on implementation, but in 90nm CMOS a delay of half a nanosecond is possible.

$$T_d = 0.5ns \tag{18}$$

The size of the gain error is a design choice. Using an ideal pipelined model in MATLAB we deduced that a gain error of $\epsilon_g = 1/2^B$ results in a 0.1dB reduction in signal-to-noise and distortion ratio (SNDR) and a spurious free dynamic range (SFDR) of 65dB. The output impedance of our current sources can then be calculated from (13)

$$R_o = 1.1M\Omega \tag{19}$$

From (15) the comparator threshold offset is

$$V_{ct} = 32mV \tag{20}$$

We now have the parameters we need for a behavioral level model. The next section verify the design equations with behavioral simulations in MATLAB and SPICE.

VII. Simulation results

The simulated ADC is a 9-bit pipelined ADC with 1.5-bits per stage. In the MATLAB model the MDAC is modeled by (7). In the SPICE model the MDAC is modeled as shown in Fig. 2 with the addition of a resistor in parallel with the current source to model the output resistance.[1]

The parameters are summarized in Table I. In all simulations we have used an input signal of -1.9dB. For an ideal converter this reduces the effective number of bits (ENOB) by 0.3-bit.

A comparison between the design equations, MATLAB model and SPICE model can be seen in Table II. There is a good match between the MATLAB model, the SPICE model, and the design equations. For SNDR and SNR there is less than 7% difference. For SFDR there is a difference of 1.3dB between SPICE and MATLAB, which corresponds to a 11% difference. We believe the reduced SFDR in SPICE simulation is due to effects not modeled in MATLAB, like switch resistance, but this has not been confirmed.

A 2048 point FFT was calculated from the outputs of the SPICE and MATLAB models to calculate the SNDR, SNR and SFDR. Coherent sampling and a Hanning window was used

[1]Both models can be downloaded from http://www.wulff.no/carsten under *Electronics*, *Tools & Scripts*, *Behavioral simulation of comparator-based switched-capacitor circuits*

TABLE I
SUMMARY OF CALCULATED PARAMETERS

Technology target	90nm CMOS
Supply voltage	1.2 V
Resolution	9 bits
Full scale input	1V
Sampling frequency	50MS/s
I_0	30μA
T_d	0.5ns
T_r	1ns
$C/2$	80fF
R_o	1.1MΩ
V_{ct}	32mV

to avoid spectral leakage of the fundamental. The FFT of the SPICE simulation is shown in (3). The FFT of the MATLAB simulation is shown in (4). The third harmonic dominate in both FFTs, but there are more spurs in the SPICE simulation.

TABLE II
RESULT OF SIMULATION

Parameter	Design Eq.	MATLAB	SPICE
ENOB	8.6dB	8.6dB	8.5dB
SNDR	53.4dB	53.5dB	53dB
SNR	53.4dB	53.8dB	53.4dB
SFDR	-	67.3dB	66dB

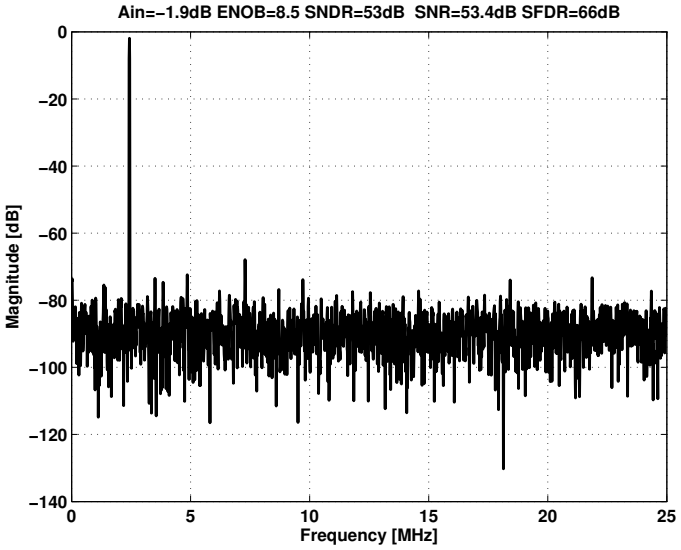

Fig. 3. 2048 point FFT of output from SPICE simulation

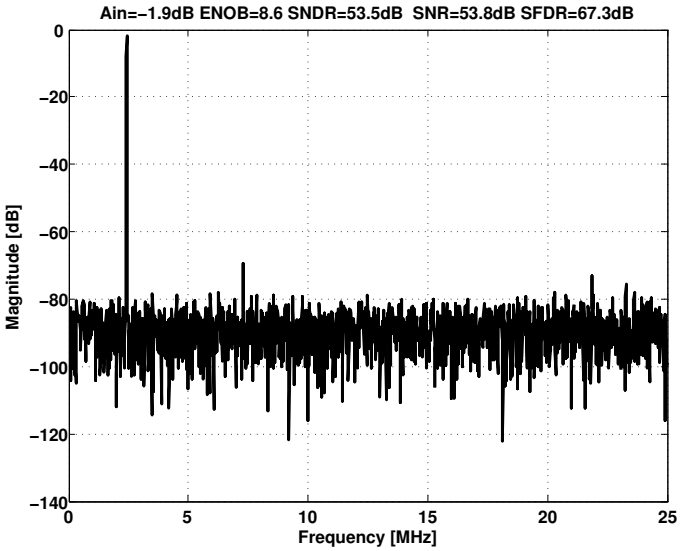

Fig. 4. 2048 point FFT of output from MATLAB simulation

VIII. CONCLUSION

Design equations are a required tool in the analog designers toolbox. In this paper we showed how one can calculate the required parameters for comparator-based switched-capacitor circuits for use in a pipelined ADC. The parameters are capacitance (C), current (I_0), comparator delay (T_d), current source output resistance (R_o) and comparator threshold (V_{ct}). The design equations were verified with behavioral simulations in SPICE and MATLAB.

REFERENCES

[1] H. Iwai, "CMOS technology-year 2010 and beyond," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 357–366, 199.

[2] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, 2005.

[3] B. R. Gregoire and U.-K. Moon, "An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain," in *ISSCC Digest of Technical Papers*, 2008, pp. 540–541.

[4] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, 2003.

[5] B. Hernes, J. Bjørnsen, T. Andersen, H. Korsvoll, F. Telsto, A. Briskemyr, C. Holdo, and O. Modsvor, "A 92.5mW 205MS/s 10b Pipeline IF ADC Implemented in 1.2V/3.3V 0.13um CMOS," in *ISSCC Digest of Technical Papers*, 2007, pp. 462–615.

[6] T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," in *ISSCC Digest of Technical Papers*, 2006, pp. 220–221.

[7] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, 2006.

[8] L. Brooks and H.-S. Lee, "A zero-crossing-based 8-bit 200MS/s pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2677–2687, 2007.

[9] T. N. Andersen, B. Hernes, A. Briskemyr, F. Telst, J. Bjrnsen, T. E. Bonnerud, and Ø. Moldsvor, "A cost-efficient high-speed 12-bit pipeline adc in 0.18-um digital cmos," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, 2005.

[10] C. Wulff and T. Ytterdal, "Design Of A 7-bit, 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In A 65nm CMOS Technology," in *Proc. NORCHIP 2007*, 2007.