Design of a 7-bit, 200MS/s, 2mW pipelined ADC with switched open-loop amplifiers in a 65nm CMOS technology

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Before we begin

- Outline
  - Low resolution ADC architectures
  - The pipelined ADC architecture
  - The open-loop amplifier
  - Simulation results
- Assumptions
  - Simulation is a good indicator of actual performance
  - The power dissipation in an ADC should be dominated by thermal noise
- Main message of this talk
  - Reducing parasitic capacitance is the key to high efficiency low resolution ADCs.
  - A pipelined ADC with switched open-loop amplifiers is an efficient architecture for low resolution ADCs
- Our contribution
  - Turning open-loop amplifiers off during sampling reduces power by 23%
  - Using 65nm CMOS technology reduces parasitic capacitance, and allows small sampling capacitors

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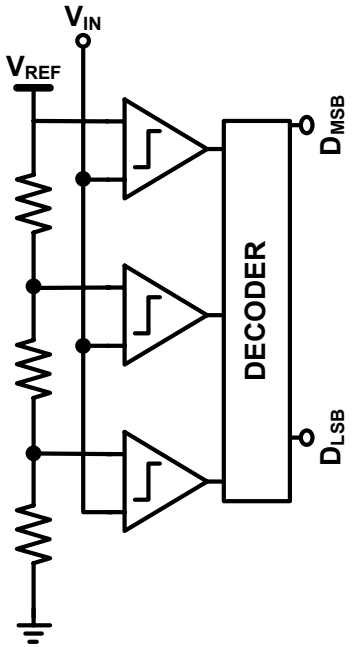
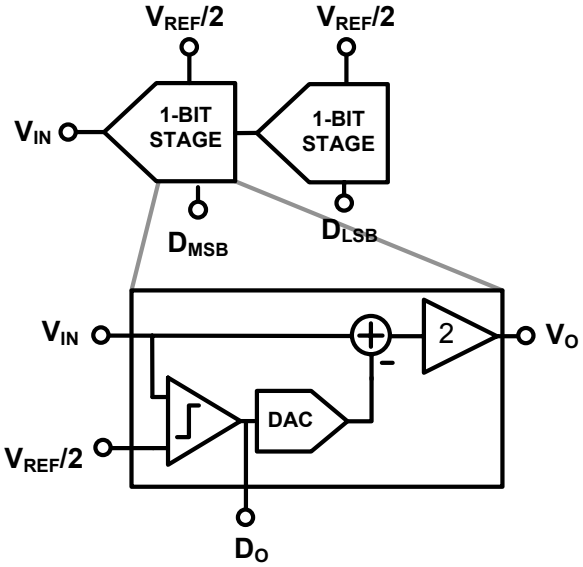
Low resolution ADC architectures

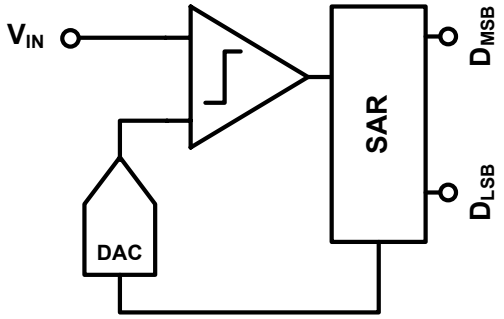
FLASH



PIPELINED



SAR



$$\overline{V_{thermal}^2} = a \times \frac{kT}{C}$$

$$C = \frac{48kT2^{2bits}}{V_{max}^2}$$

	Speed	Power	Power/Speed	Input Cap. 6-bit
FLASH	1	2^N	2^N	640fF
PIPELINED	1/b	c x N	bc x N	d x 10fF
SAR	1/N	1	N	10fF

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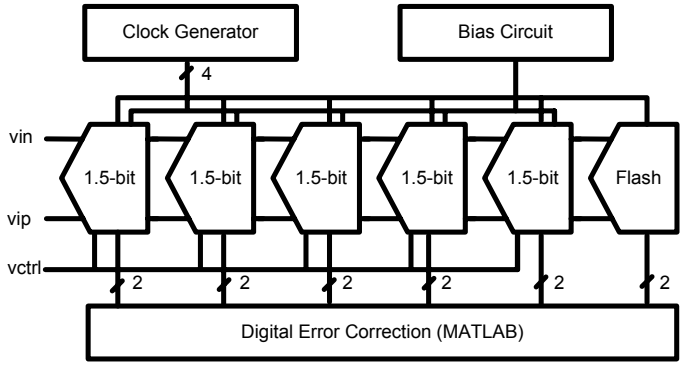
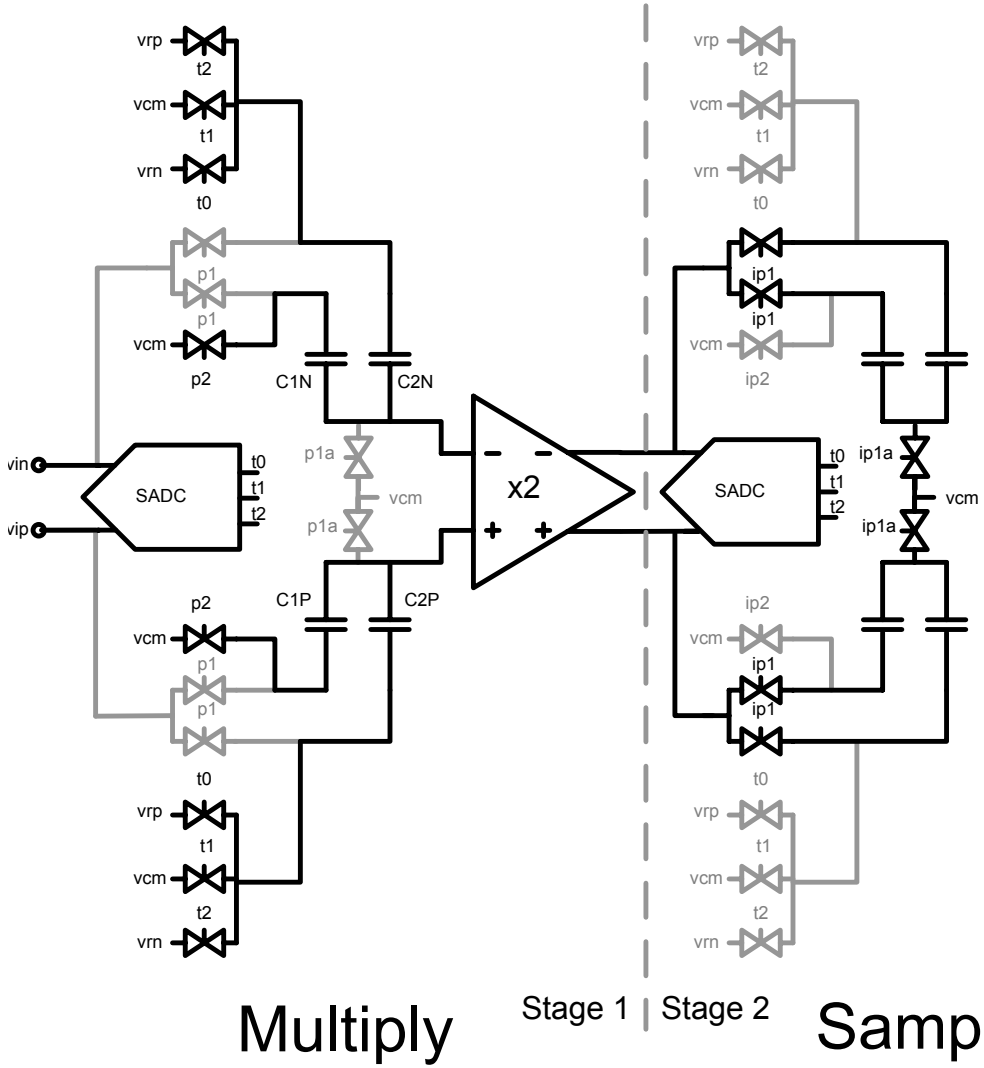
Carsten Wulff et al, "Design of a 7-bit, 200MS/s, 2mW pipelined ADC with switched open-loop amplifiers in a 65nm Technology"

Pipelined Architecture



Highlights:
- 65 nm LP CMOS Technology
- Switched capacitor implementation
- 50fF sampling capacitors
- Six 1.5 bit stages + 1.5 bit Flash
- Four phase clock generator
- Switched open-loop amplifiers
- Transmission gates as switches
- Digital error correction in MATLAB

Not Included:
- Reference buffers
- Input buffers and antialias filter



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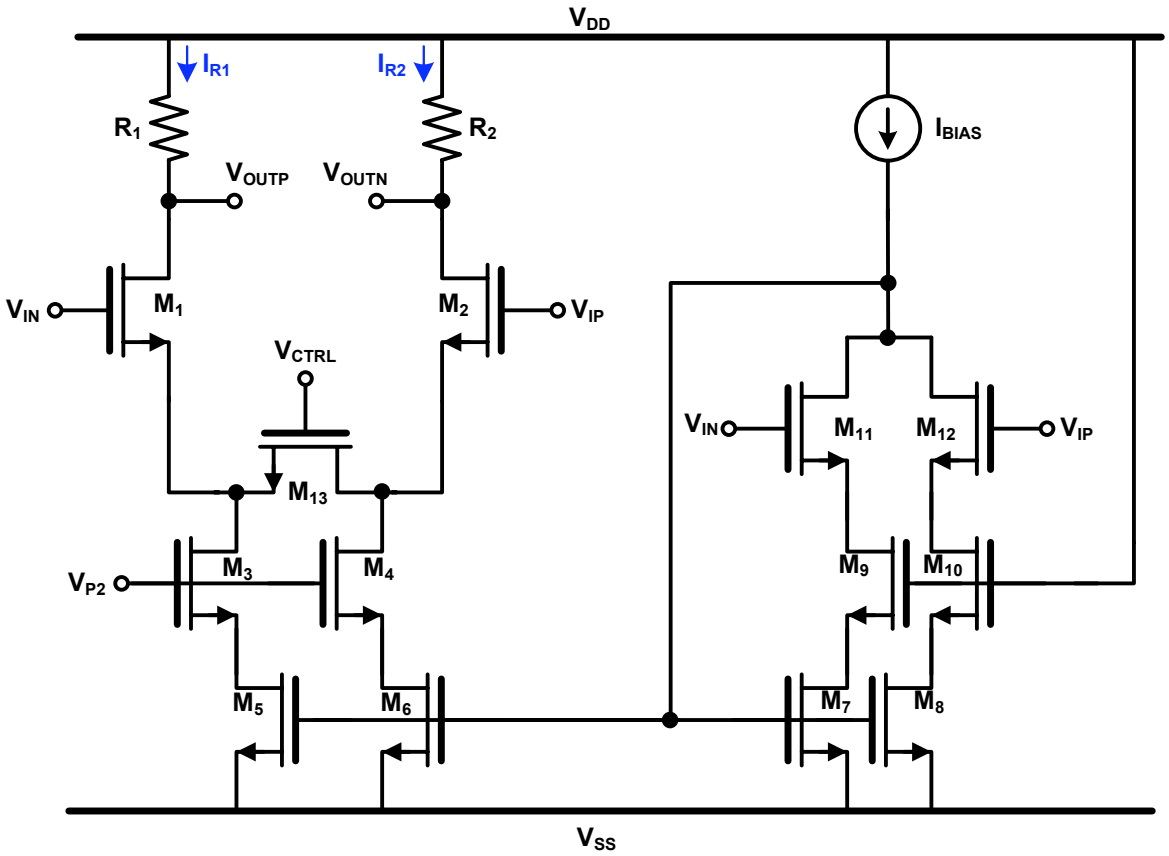
Open-loop amplifier

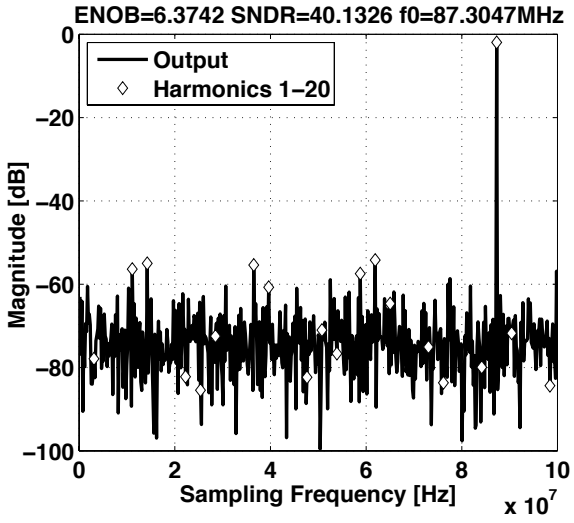
- Based on Shen07 [2]
- Resistors and I_{BIAS} set the output common mode
- Replica bias keeps $I_{R1} + I_{R2} = 2\ I_{BIAS}$
- Source degeneration (M_{13}) provide gain control
- Switches turn off amplifier when it is not needed
- < 7 bit linearity without calibration

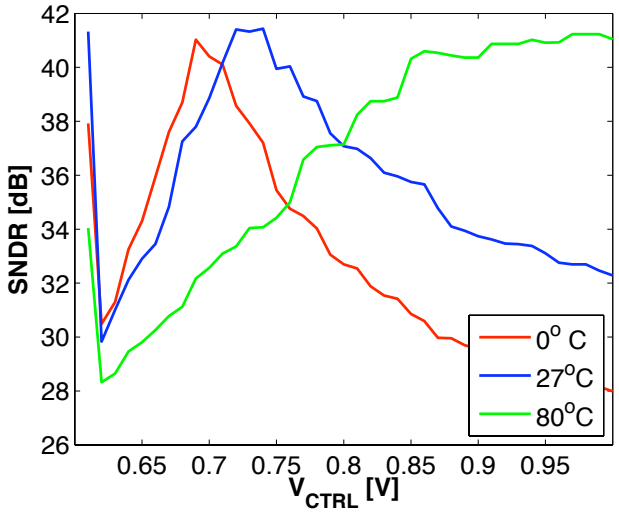


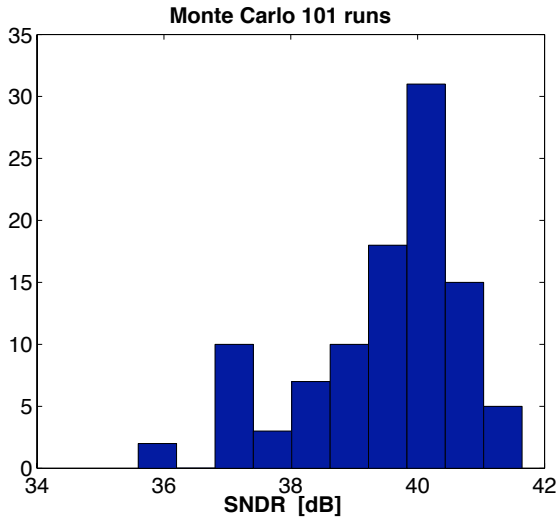
$$V_{CM} = V_{DD} - I_{TOT}(R_1+R_2)/2$$

$$A_o = \frac{g_{m1}R_1}{1 + \frac{g_{m1}}{2g_{ds13}}}$$

Results







	Arch.	Tech. [nm]	TI	Power [mW]	ENOB [bits]	Fs [MS/s]	Thermal FOM Smaller is better
This work	Pipelined w/OL	65	1	2	~ 6.3	200	~ 1.6 fJ/step
Chen06 [1]	Asynch. SAR	130	2	5.3	5.3	600	5.7 fJ/step
Shen07 [2]	Pipelined w/OL	180	2	105	5.35	800	59 fJ/step

$$FOM = \frac{P_{diss}}{2^{2bits} f_s}$$

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Conclusion

- Reducing parasitic capacitance is the key to high efficiency low resolution ADCs. Use technologies with low parasitic capacitance, like 65 nm CMOS technologies
- A pipelined ADC with switched open-loop amplifiers is an efficient architecture for low resolution ADCs
- Turning open-loop amplifiers off during sampling reduces power dissipation

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References

1. S.-W. M. Chen and R. W. Brodersen, “A 6-bit 600ms/s 5.3mw asynchronous adc in 0.13-µm cmos,” IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2669–2679, 2006.
2. D.-L. Shen and T.-C. Lee, “A 6-bit 800ms/s pipelined a/d converter with open-loop amplifiers,” IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 258–268, 2007.

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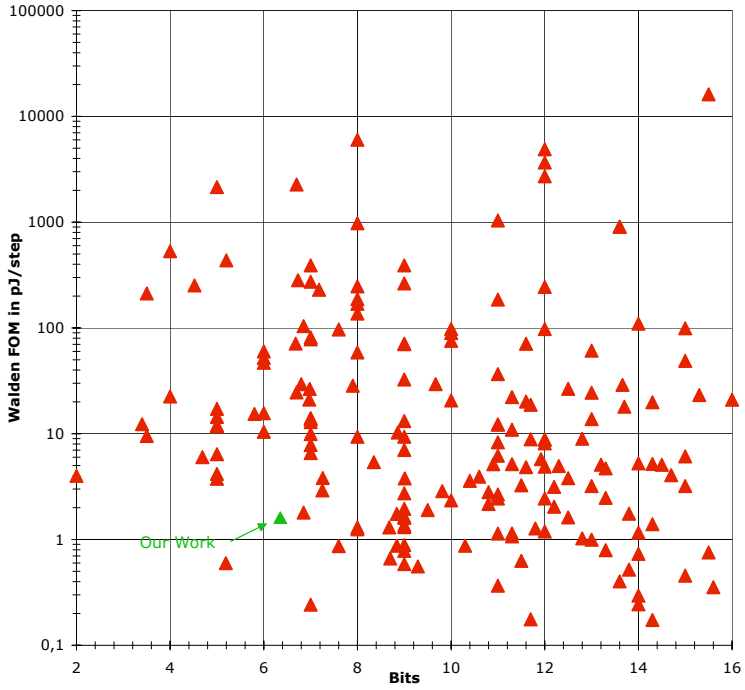
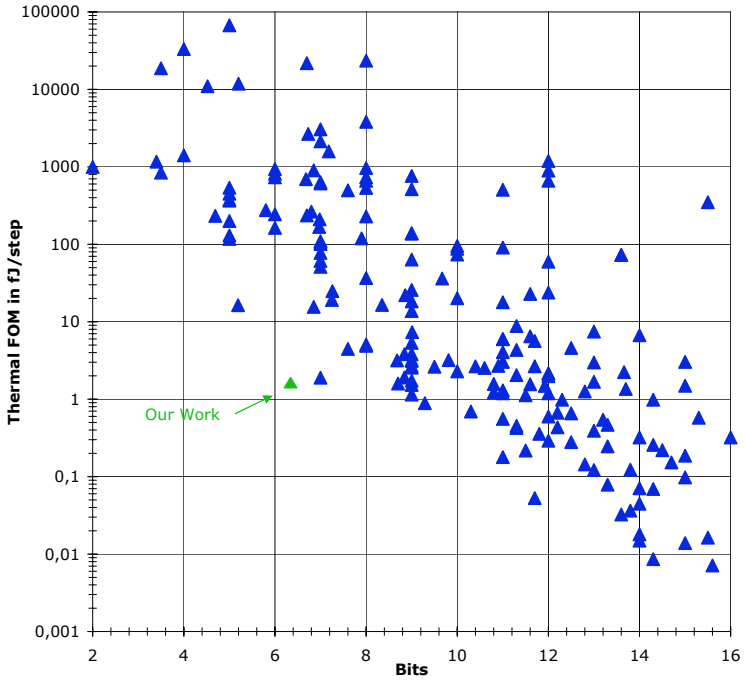
ADC Figure of Merit

Walden FOM



Thermal FOM



$$FOM = \frac{P_{diss}}{2^{bits} f_s} \qquad C = \frac{48kT2^{2bits}}{V_{max}^2} \qquad FOM = \frac{P_{diss}}{2^{2bits} f_s}$$

1 bit → double the power

1 bit → four times the power

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Thermal noise power

- Thermal noise power in switched-capacitor circuits is given by

$$\overline{V_{thermal}^2} = a \times \frac{kT}{C}$$

- Sampling capacitor needed to achieve thermal noise power of one fourth of the quantization noise power is given by

$$C = \frac{48kT2^{2bits}}{V_{max}^2}$$

Thermal noise limited: Double the accuracy → Four times the power

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Parasitic Capacitance

- Parasitic Capacitance: Any capacitance not required by the operation of the circuit.
- Parasitic capacitance in current nanoscale technology can exceed 10fF per node

- Required input capacitance for thermal noise power at one fourth the quantization noise power at 6-bit level

	$0^{O}C$	$80^{O}C$
V_{MAX} = 0.4 V	4.6fF	6fF

Difficult to get input capacitance down minimum required at 6-bit level
Use technologies with low parasitic capacitance like 65nm CMOS

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