0.8V 1GHz Dynamic Comparator in Digital 90nm CMOS Technology

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Abstract:

The design of a 0.8V 1GHz dynamic comparator in digital 90nm CMOS technology is presented. The work will show that low voltage, low power and high speed analog circuits are feasible in nano-scale CMOS technologies. The dynamic comparator dissipates a maximum of 222μW at 1GHz clock frequency with 100fF capacitive load and 0.8V supply voltage. This is lower than comparable results.

1.   Introduction

One of the factors driving the downscaling of CMOS technology is the ever present drive for price-per-performance of digital circuits. The minimum dimensions get smaller and maximum supply voltages are reduced due to reliability issues [1]. Since digital circuits are the driving force of silicon technology, analog circuit designers often have to work in digital CMOS processes. The reduction in supply voltage is not necessarily followed by an equal reduction in threshold voltage, which limits the available voltage headroom [2]. These nano-scale CMOS technologies offer many challenges that have been discussed in previous publications, among others [1-3]. The challenges have, in some cases, brought success to simpler topologies [4] that have shown some of the advantages of nano-scale CMOS for analog circuits. One advantage of scaling down is the increased speed that follows. It can be shown that the unity gain frequency (f_{UG}) of a transistor is proportional to the effective gate voltage (V_{GT}) over the square of the length (L) of a transistor as given by (1) [2].

$$f_{UG} \propto \frac{V_{GT}}{L^2} \qquad (1)$$

Thus the trend will be that shorter lengths bring higher speeds.

Dynamic comparators are a class of circuits often used in pipeline analog to digital converters (ADCs) [5]. As the name suggests a pipeline ADC consists of multiple stages. It is common to extract at least 1.5-bits in each stage. The 1.5-bits per stage stem from a digital error correction algorithm that requires a certain redundancy in the number of bits. With the digital error correction comparators in each stage can have quite large offset. Using 1.5-bits per stage one can tolerate a comparator

offset of up to $\pm V_{REF}/4$, where V_{REF} is the high reference voltage minus the common mode voltage. In general, the comparators can tolerate an offset up to $\pm V_{REF}/2^b$ for a b-bit stage [6]. Using dynamic comparators may reduce the architectural complexity and reduce power dissipation, but tight control over variations and mismatch must be exercised to ensure that offset and other errors are kept within the allowed limits. Architectures that reduce mismatch have been presented [6]. In this paper, we describe a dynamic comparator that is a modification of MOSFET-only fully-differential dynamic comparator presented in [7]. We will first describe the architecture and operation of the comparator before we present the design in 90nm CMOS and simulation results.

2.   Dynamic comparator architecture

The circuit can be seen in Figure 1. In [7] they used a clock booster to supply a higher voltage to M1-M4 than the supply voltage. To avoid any reliability concerns that may come with boosted voltages we have replaced the clock booster with a single transistor M5. The comparator has two phases; Reset and Latch. In the Reset phase the latch, shown by the back to back inverters, is shorted to ground through M6 and M7. To stop current flowing through the shorted inverters M5 is turned off. Notice that both operations are accomplished by a transition on CLK from low to high. This resets the output of the comparator to zero and place INV1 and INV2 in a known state. For the comparator to work properly it is important that INV1 and INV2 are reset to a known state, any unintentional imbalance between the two inverters might tip the comparator towards one side. When the clock goes from high to low we enter the Latch phase. In this phase the inverters are connected in a positive feedback loop. What way the latch will swing is controlled by an intentional imbalance in the supply to the inverters. This imbalance is controlled by the transistors M1-M4. Depending on their gate voltages transistors M1-M4 have variable on-resistance. For the moment we will ignore transistors M2 and M3. If M1 and M4 are matched, their on-resistances will be the equal when the differential input voltage (V_{INPUT}) is zero (VIN = VIP). When V_{INPUT} is negative (VIN > VIP) M4 will turn more off, and the resistance in M1 will be lower than resistance in M4. Thus INV1 will be slightly faster than INV2, and the comparator will settle to VOP equals zero and VON equals one. The opposite will occur if the V_{INPUT} is positive (VIP > VIN). Notice that this comparator does not need multiple clocks or inverted

clocks, one clock signal is sufficient to trigger transition from one phase to another and back again.
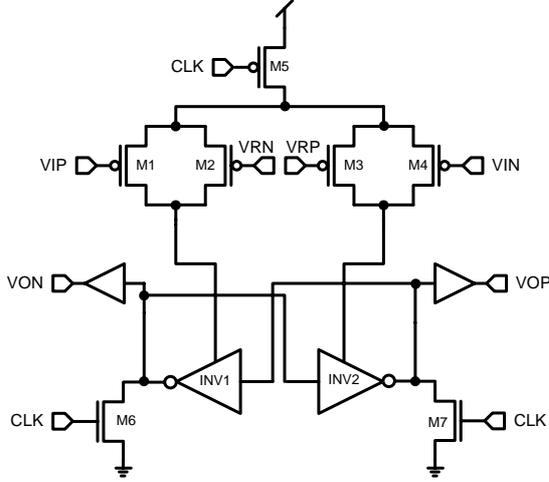
Figure 1 Dynamic comparator

As stated, with M2 and M3 ignored the comparator has a threshold at $V_{INPUT} = 0$. However, in a 1.5-bit pipeline stage we need two comparators with the thresholds given by eqs. (2) and (3) [6]. The transistors M2 and M3 serve to offset the threshold of the comparator. They add small amounts of current to the two branches and intentionally tip the balance of the comparator. Ideally we would scale M2 and M3 to one fourth of the width of M1 and M4. However, as we will se later, this is different in a real process.

$$V_{INPUT} = +\frac{1}{4}V_{REF} \qquad (2)$$

$$V_{INPUT} = -\frac{1}{4}V_{REF} \qquad (3)$$

We have two reference voltages, high and low. These are common mode plus V_{REF} and common mode minus V_{REF}, respectively. With the high and low reference voltages connected to VRP and VRN, respectively, the threshold will be set at (2). If we reverse the connections to VRP and VRN we set the threshold at (3).

The boundary conditions for the inverters play an important role in deciding which way the comparator swings. If we have large difference in e.g. the capacitive load at the output of the inverters the comparator might swing the wrong way. Therefore, we keep the load controlled by using two matched buffers at the output of the inverters. We have chosen a high reference at 0.6V and a low reference at 0.2V. The common mode is set at 0.4V. Thus, the maximum allowable offset in this work is $\pm V_{REF}/4 = \pm 0.2V/4 = \pm 50mV$. Simulations will show that the comparator stays within this limit.

Mismatch between transistors can influence the offset of the comparator. Mismatch of MOSFET transistors can be reduced by increasing the area of the transistor [8]. We tried to keep transistor areas as large as possible in order to reduce mismatch, while small enough to keep capacitances low. All transistors have a length of 0.1μm to maximize the speed, according to (1). All PMOS devices have a width of 3μm and all NMOS devices have a width of 1.2μm as seen in Table 1. Devices are kept at the same width to simplify layout to maximizing the matching [9]. Notice that the effective width, width x Number of Unit Devices in parallel (NUD), of M1 and M2 does not correspond to a scaling of one-fourth. In the 90nm process we are using a scaling of eight was necessary to keep the threshold at the reasonable level. M6 and M7 are the twice the effective width of the NMOS transistors in the inverters.

Transistor	Width (μm)	NUD[1]
M1 & M4	3.0	16
M2 & M3	3.0	2
M5	3.0	84
M6 & M7	1.2	2

Table 1 Transistor widths and fingers
[1]NUD: Number of Unit Devices in parallel

3. Simulation Results

Some of the key parameters for this dynamic comparator are offset, delay and power dissipation. The offset needs to be within plus/minus one-fourth of the reference voltage, which in our case corresponds to ±50mV. We aimed for a speed of 1GHz at 0.8V. This corresponds to a maximum delay of 500ps from CLK goes low to output is valid. Remember that the comparator has two phases; Reset and Latch, they need 500ps each at 1GHz clock frequency with a 50% duty cycle. We have not considered other duty cycle arrangements.

Since we were primarily considering high speed and low voltage, we did not set any requirements for power dissipation. However, dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by:

$$P = f\,C\,V_{DD}^{2} + V_{DD}I_0 \qquad (4)$$

Where f is the output frequency, V_{DD} is the supply voltage, C is the output capacitance and I_0 is the average leakage current [10]. With a low supply voltage and limited capacitance we anticipated reasonable power consumption.

Simulations were performed in five process corners; Fast, Typical, Slow and cross corners (fast NMOS, slow PMOS and visa versa). We also ran three temperature

corners (-40°, 0°, 85°) for each process corner. In addition, Monte Carlo simulations were performed to simulate the effect of mismatch. All transistors included a model of gate leakage current. A capacitive load of 100fF was used at the output of the buffers in all simulations. Each parameter (offset, delay and power dissipation) was extracted in each of the corners. Typical values were extracted from typical process corner. The standard deviation (σ) for power dissipation and offset was extracted from a Monte Carlo simulation. For offset it was around 3 mV for both high and low threshold. For power dissipation the standard deviation was negligible. We subtracted 3σ from the minimum value and added 3σ to the maximum value of offset and power dissipation. Table 2 shows the results for comparator offset and power dissipation including 3σ. The offset is within ±25mV which is well below the required ±50mV. The maximum power dissipation was 222µW, almost half of this was dissipated in the output buffers. As previously stated we have used a similar architecture to that of [7]. They achieved 100µW with 200fF at 50Msamples/s and 1V in a 0.25µm CMOS technology. Since most of the power dissipation in this architecture is dynamic we can use (4) to compare the two results. If we scale the results from [7] to 1GHz with 100fF and 0.8V we get a power dissipation of 640µW. Thus, a maximum power dissipation of 222µW at 1GHz with 100fF and 0.8V can be considered reasonable.

Simulating delay in a comparator requires that one choose the input signal with care. It can be shown that the delay of latched comparators becomes large when the differential input voltage is close to threshold [9]. We simulated the delay around the threshold by applying a differential ramp at the input from 20mV above the ideal threshold to 20mV below the ideal threshold using 200 clock periods running at 1GHz. The change in input from one clock period to the next was around 200µV. It is difficult to know exactly where the threshold of the comparator is. We therefore used the delay of the second pulse after the comparator switched states. By doing this we know we never measure delay exactly at the threshold, but always within 200µ - 400µV away from the threshold. As with offset and power dissipation, a Monte Carlo simulation was performed to get the σ of the delay. The σ of the delay decreased as we moved away from the threshold. The standard deviation of the delay for the first pulse after threshold was up to 30-50ps for high and low thresholds, most of which we believe is due to varying distance to threshold when the comparator latches. The σ of the delay for the second pulse was below 10ps, it is this σ that has been used in Table 2. In the worst corner and including 3σ variation in delay due to mismatch, the comparator has less than 400ps delay. This would give us a maximum clock frequency of 1.25GHz, but allowing for a safety margin we choose 1GHz as maximum.

If the differential input voltage is closer than ±200µV to the threshold, less than what was used in simulation, there is a chance of metastability. Metastability is when the comparator has larger delay than the available settling time. A detector for metastability can be inserted after the comparator [11]. A XOR port connected to VON and VOP, with delay much smaller than the comparator, will give a one if there is no metastability and zero if there is metastability. This is ensured by the reset to zero of both outputs in the Reset phase. In a case of metastability one can arbitrarily choose output state of the comparator since one knows that the input is close to threshold, much closer than the required ±50mV. However, when using a metastability detector one must make sure that the pull-down delay of Reset plus delay of the detector is less than half the clock period. In this design the pull-down delay in Reset was below 200ps. We have not yet considered effects of layout parasitics.

Parameter	Min	Typ	Max	Unit
Offset (High threshold)	-22.5	9	15	mV
Offset (Low threshold)	-16	8.5	22	mV
Power diss.@1GHz	180	193	222	µW
Delay	80	186	< 400	ps

Table 2 Offset, power dissipation and delay

4. Future work

The comparator is scheduled for production in a digital 90nm CMOS technology during fall of 2005. The main purpose of the prototype is to verify the rather small variations due to process variation and mismatch seen in simulations. If the prototype confirms what has been seen in simulations the comparator will be used in scheduled high performance ADCs.

5. Acknowledgements

6. Conclusion

The design of a 0.8V 1GHz dynamic comparator in digital 90nm CMOS technology has been presented. The work shows that low voltage, low power and high speed analog circuits are feasible in nano-scale CMOS technology. The dynamic comparator dissipates a maximum of 222µW at 1GHz clock frequency with 100fF capacitive load at a supply voltage of 0.8V which is lower than comparable results. Table 3 shows a summary of simulation results.

Offset	$< \pm 25\text{mV}$
Clock Frequency	$> 1\text{GHz}$
Power dissipation	$< 222\mu\text{W}$
Supply voltage	0.8 V
Clock signals	1
High reference	0.6V
Low reference	0.2V
Common mode	0.4V

Table 3 Summary of simulation results

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